CS-97-110/112

AF 2814

February 15, 2002

#19/Appeal Brief 4-1-02 Hayes

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, NY 12603

Subject: Serial No. 09/186,388 11/05/98

B. LEE et al.

"N TYPE IMPURITY DOPING USING IMPLANTATION OF P_2^+ IONS OR As_2^+ IONS" (AS AMENDED)

Grp. Art Unit: 2814 G. PERALTA

APPEAL BRIEF

Dear Sir:

In response to the Final Rejection of Claims 1-28 dated November 7, 2001 for the above referenced Application for Patent please accept this Appeal Brief:

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on February 25, 2002.

Name George O. Saile, Reg #19,572

Signature George O. Saile

Date 2/25/02

The Commissioner is hereby authorized to charge payment of the fee of $320.00 associated with this communication to Deposit Account No. 19-0033. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

George O. Saile

George O. Saile, Reg. No. 19,572

REAL PARTY IN INTEREST

The real party in interest is the assignee, Charter Semiconductor Manufacturing Company, Ltd., 60 Woodlands, Industrial Park D, Street 2, Singapore 738406, Singapore. An assignment has been recorded for this case.

RELATED APPEALS AND INTERFERENCES

There are no additional Appeals or Interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal of the Subject Application for Patent.

STATUS OF CLAIMS

Claims 1-28 are pending in the Patent Application and have been rejected. Appendix A has Claims 1-28 in numerical sequence.

STATUS OF AMENDMENTS

There are no pending amendments.

SUMMARY OF THE INVENTION

INTRODUCTION

Ion implantation is used frequently in the manufacture of integrated circuits. Ion beams are used to implant impurities into semiconductor wafers to provide doping for source/drain regions, polysilicon electrode patterns, and the like. In ion beam implantation the beam energy and ion density are chosen to provide the desired impurity profile after implantation. One problem encountered as device geometries become smaller and source/drain junction depths become smaller is that the ion beam energy must become lower, in some cases less than 10 KeV. At these low energies it is difficult to obtain sufficient ion beam density resulting in lower throughput rates and increased implant cycle times, which directly impact cost. In addition the ion sources are stressed by these conditions and must be replaced with increased frequency.

It is a principle objective of this invention to provide a method of implanting phosphorous in source/drain regions using ion beam implantation with increased beam energy in applications having very shallow junctions.

It is another principle objective of this invention to provide a method of implanting arsenic in source/drain regions using ion beam implantation with increased beam energy in applications having very shallow junctions.

It is another principle objective of this invention to provide a method of implanting phosphorous in polysilicon electrodes using ion beam implantation with increased beam energy in applications having very shallow junctions.

It is another principle objective of this invention to provide a method of implanting arsenic in polysilicon electrodes using ion beam implantation with increased beam energy in applications having very shallow junctions.

These objectives are achieved by using ion sources such as solid phosphorous, phosphine gas, solid arsenic, or SDS arsine in the ion beam apparatus. The magnetic analyzer of the ion beam apparatus is then adjusted to select either the P_2^+ or the As_2^+ isotopes for the ion beam. These ion beams can then be implanted using energies of 20 KeV or greater.

APPLICANTS CONTRIBUTION TO THE ART

The invention is described with reference to Figs. 1-4 of the Drawings. Fig. 1 shows a schematic view of an ion beam apparatus. Different ion beam systems may differ from the one shown and described herein but certain key features will be common to all ion beam systems. The ion beam apparatus has an ion source 10 which uses a small accelerating voltage to inject an ion beam 24 into an evacuated enclosure 12. Ion sources can be solid materials or gasses such as solid phosphorous, phosphine gas, solid arsenic, or SDS arsine.

Referring again to Fig. 1, the beam then enters a magnetic analyzer 14 which is adjusted to select particles with a particular mass to charge ratio for the beam 25 exiting the magnetic analyzer. For the example of an ion source 10 using solid phosphorous or phosphine gas the magnetic analyzer 14 is adjusted to select singly charged P_2 ions which have a mass of 62 atomic mass units and a charge equal to the charge of a single electron. These ions will be designated as P_2^+ ions. Solid phosphorous or phosphine gas provide an abundance of P_2 isotopes. Solid arsenic or SDS arsine can also be used as the ion source 10. In this case the magnetic analyzer 14 is adjusted to select singly charged As_2 ions which have a mass of 150 atomic mass units

and a charge equal to the charge of a single electron. These ions will be designated as As_2^+ ions. Solid arsenic or SDS arsine provide an abundance of As_2 isotopes.

As shown in Fig. 1, the ion beam 25 exiting the magnetic analyzer 14 is then directed through a voltage accelerator/decelerator 16 where the selected beam energy is imparted to the ion beam 25. The ion beam 26 exiting the voltage accelerator/decelerator 16 passes through a scanning system 18 which directs the ion beam. The ion beam exiting the scanning system 18 passes through an energy filter 52, to provide improved energy uniformity, and a plasma flood gun 54, to neutralize any charge buildup on the wafer during ion implantation. The ion beam 27 exiting the plasma flood gun 54 is directed, by the scanning system 18, to the proper location on an integrated circuit wafer 30 which is attached to a wafer holder 20. A coupling mechanism 22 attaches the wafer holder 20 to the evacuated enclosure 12. In this manner the ion beam 27 exiting the scanning system can be used to implant impurities into source/drain regions or into polysilicon electrodes.

Fig. 2 shows a part of the wafer 30 which is held in place by the wafer holder in the evacuated enclosure. The wafer comprises a substrate, in this example a P type silicon substrate, having field oxide isolation regions 34

and a gate oxide layer 36. A gate electrode 40 is formed on the gate oxide layer 36. The ion beam 27 is used to implant impurities into the source/drain regions 38. In this example the ion beam 27 is a P_2^+ ion beam having a beam density of between about 4 X 10^{14} and 6 X 10^{14} ions/cm^2 and a beam energy of between about 20 and 48 KeV. The beam density used is one half that required for a beam of P^+ ions because two phosphorous atoms are implanted for every P_2^+ ion implanted. The beam energy is double that would be required for a beam of P^+ ions because each of the P_2^+ ions have two phosphorous atoms. After the implantation the wafer is rapidly annealed at an anneal temperature of between about 900°C and 1100°C for between about 10 and 20 seconds. This method produces shallow source/drain regions 38 using beam density and energy levels which maintain good throughput and source life.

Fig. 3 also shows a part of the wafer 30 which is held in place by the wafer holder in the evacuated enclosure. The wafer comprises a substrate, in this example a P type silicon substrate, having field oxide isolation regions 34 and a gate oxide layer 36. A polysilicon gate electrode 40 is formed on the gate oxide layer 36. The ion beam 27 is used to implant impurities into the polysilicon gate electrode 40. In this example the ion beam 27 is a P_2^+ ion beam having a beam density of between about 4 X 10^{14} and

6 X 10^{14} ions/cm^2 and a beam energy of between about 20 and 48 KeV. The beam density used is one half that required for a beam of P^+ ions because two phosphorous atoms are implanted for every P_2^+ ion implanted. The beam energy is double that would be required for a beam of P^+ ions because each of the P_2^+ ions have two phosphorous atoms. After the implantation the wafer is annealed at an anneal temperature of between about 900°C and 1100°C for between about 10 and 20 seconds. This method produces good conductivity for the polysilicon gate electrode 40 using beam density and energy levels which maintain good throughput and source life.

Referring again to Fig. 2, an ion beam 27 of As_2^+ ions can be used to implant impurities into the source/drain region 38. The wafer comprises a substrate, in this example a P type silicon substrate, having field oxide isolation regions 34 and a gate oxide layer 36. In this example the ion beam 27 is an As_2^+ ion beam having a beam density of between about 4 X 10^{14} and 6 X 10^{14} ions/cm^2 and a beam energy of between about 20 and 48 KeV. The beam density used is one half that required for a beam of As^+ ions because two arsenic atoms are implanted for every As_2^+ ion implanted. The beam energy is double that would be required for a beam of As^+ ions because each of the As_2^+ ions have two arsenic atoms. After the implantation the wafer is annealed at an anneal temperature of between about 900°C and

1100°C for between about 10 and 20 seconds. This method produces shallow source/drain regions 38 using beam density and energy levels which maintain good throughput and source life.

Referring again to Fig. 3, an ion beam 27 of As_2^+ ions can be used to implant impurities into the polysilicon gate electrode 40. The wafer comprises a substrate, in this example a P type silicon substrate, having field oxide isolation regions 34 and a gate oxide layer 36. In this example the ion beam 27 is an As_2^+ ion beam having a beam density of between about 4 X 10^{14} and 6 X 10^{14} ions/cm^2 and a beam energy of between about 20 and 48 KeV. The beam density used is one half that required for a beam of As^+ ions because two arsenic atoms are implanted for every As_2^+ ion implanted. The beam energy is double that would be required for a beam of As^+ ions because each of the As_2^+ ions have two arsenic atoms. After the implantation the wafer is annealed at an anneal temperature of between about 900°C and 1100°C for between about 10 and 20 seconds. This method produces good conductivity for the polysilicon gate electrode 40 using beam density and energy levels which maintain good throughput and source life.

Fig. 4 shows the AMU, atomic mass unit, spectrum for a source of solid phosphorous in an ion beam system using a beam energy of 30 KeV. The spectrum clearly shows a first beam current peak 44 at 31 atomic mass units and a second beam current peak 46 at 62 atomic mass units. This curve clearly shows that when the magnetic analyzer is adjusted to select phosphorous ions having 62 atomic mass units there is ample beam current available.

ISSUES

Claims 1-28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Current (U.S. Pat. No. 5,155,369) in view of Aitken (U.S. Pat. No. 4,578,589).

GROUPING OF THE CLAIMS

Claims 1-14, rejected under 35 U.S.C. § 103(a) as being unpatentable over Current in view of Aitken, will be argued as a group and stand or fall together.

Claims 15-28, rejected under 35 U.S.C. § 103(a) as being unpatentable over Current in view of Aitken, will be argued as a group and stand or fall together.

Arguments for why Claims 1-14 and Claims 15-28 should be separately patentable will be given in the ARGUMENT section of this Appeal Brief

ARGUMENT

GROUPING OF THE CLAIMS

Claims 1-14 describe methods of forming source/drain regions of a semiconductor integrated circuit wafer using ion implantation of P_2^+ or As_2^+ ions. Claims 15-28 describe methods of doping polysilicon electrodes using ion implantation of P_2^+ or As_2^+ ions. The source/drain regions of a semiconductor integrated circuit wafer are formed in the body of a single crystal semiconductor wafer. The polysilicon electrode is formed of poly-crystalline silicon material. The requirements of doping source/drain regions are different from the requirements of doping polysilicon electrodes because the crystalline structure of single crystal material is different from the crystalline structure of poly-crystalline material. It is believed that Claims 1-14, describing doping methods for source/drain regions, are separately patentable from Claims 15-28, describing doping methods for polysilicon electrodes, because of the different crystalline structure of the

source/drain regions and the polysilicon electrodes.

Rejection of Claims 1-14 under 35 U.S.C. § 103(a) as being unpatentable over Current (U.S. Pat. No. 5,155,369) in view of Aitken (U.S. Pat. No. 4,578,589).

Claims 1-14 describe methods of doping source/drain regions in an integrated circuit wafer using a single ion implantation step using implantation of either P_2^+ ions, Claims 1-7, or As_2^+ ions, Claims 8-14. A key feature of the doping methods described in Claims 1-14 is that the source/drain regions are doped using a single ion implantation step.

The Examiner has argued that Current teaches all of the limitations of the claims except the placing a phosphorous, Claims 1-7, or arsenic, Claims 8-14, ion source in the ion implant apparatus. The Examiner has argued that Aitken teaches an ion implantation apparatus using solid phosphorous source or solid arsenic sources.

We respectfully disagree that Current teaches all the limitations of the claims except the placing a phosphorous or arsenic ion source in the ion implant apparatus for the following reasons. Current describes a two step ion implantation method while Claims 1-14 describe

single step ion implantation methods. In first sentence of the Abstract Current describes an "implantation process in which a first dose of ions is implanted to produce a damaged layer through which a second dose of implant ions is directed." In one embodiment described by Current the first step implants a light dose of ions at an angle of 5-7 degrees away from the normal to the surface of the substrate. The second step implants a much larger dose directed along the normal to the surface of the substrate, see column 3, lines 35-60. In a variant of this embodiment the implantation energy is much smaller in the first implantation step than in the second implantation step, see column 4, lines 7-9. In another embodiment described by Current the first implantation step is broken into a pair of substeps. In the first substep the ions are incident at an angle A with respect to the normal to the surface of the substrate. In the second substep the ions are incident at an angle -A with respect to the normal to the surface of the substrate, see column 4, lines 54-60.

It is believed that the single step ion implantation methods of Claims 1-14 are significantly different from the two step ion implantation methods taught by Current. The invention of Aitken does not make the single step ion implantation method of Claims 1-14 an obvious extension of the multiple step ion implantation

methods taught by Current.

Rejection of Claims 15-28 under 35 U.S.C. § 103(a) as being unpatentable over Current (U.S. Pat. No. 5,155,369) in view of Aitken (U.S. Pat. No. 4,578,589).

Claims 15-28 describe methods of doping polysilicon electrodes using a single ion implantation step using implantation of either P_2^+ ions, Claims 15-21, or As_2^+ ions, Claims 22-28. A key feature of the doping methods described in Claims 15-28 is that the polysilicon electrodes are doped using a single ion implantation step.

The Examiner has argued that Current teaches all of the limitations of the claims except the placing a phosphorous, Claims 15-21, or arsenic, Claims 22-28, ion source in the ion implant apparatus. The Examiner has argued that Aitken teaches an ion implantation apparatus using solid phosphorous source or solid arsenic sources.

We respectfully disagree that Current teaches all the limitations of the claims except the placing a phosphorous or arsenic ion source in the ion implant apparatus for the following reasons. Current describes a two step ion implantation method while Claims 15-28 describe

single step ion implantation methods. In addition Current describes methods of doping by implanting dopant ions into a crystal lattice; see column 3, lines 35-53; while Claims 15-28 describe doping polysilicon electrodes.

In first sentence of the Abstract Current describes an "implantation process in which a first dose of ions is implanted to produce a damaged layer through which a second dose of implant ions is directed." In one embodiment described by Current the first step implants a light dose of ions at an angle of 5-7 degrees away from the normal to the surface of the substrate. The second step implants a much larger dose directed along the normal to the surface of the substrate, see column 3, lines 35-60. In a variant of this embodiment the implantation energy is much smaller in the first implantation step than in the second implantation step, see column 4, lines 7-9. In another embodiment described by Current the first implantation step is broken into a pair of substeps. In the first substep the ions are incident at an angle A with respect to the normal to the surface of the substrate. In the second substep the ions are incident at an angle -A with respect to the normal to the surface of the substrate, see column 4, lines 54-60.

In the description of the methods of Current significant discussion is devoted to the crystalline damage during a first implant step and the effect of that damage during a second implant step. The crystalline structure of polysilicon electrodes described in Claims 15-28 is different from the crystalline structure described by Current.

It is believed that the single step ion implantation methods of Claims 15-28 are significantly different from the two step ion implantation methods taught by Current. It is also believed that the doping of the polysilicon electrodes of Claims 15-28 is significantly different from the doping of the crystalline structure described by Current. The invention of Aitken does not make the single step ion implantation methods for doping polysilicon electrodes of Claims 15-28 an obvious extension of the multiple step ion implantation methods taught by Current.

SUMMARY

Claims 1-14 and Claims 15-28 distinguish patentably from the references and should be allowed. Applicant requests that the Board of Appeals reverse the final rejection of Claims 1-14 under 35 U.S.C. § 103(a) as being unpatentable over Current (U.S. Pat. No. 5,155,369) in view of Aitken (U.S. Pat. No. 4,578,589). Applicant further requests that the Board of Appeals reverse the final rejection of Claims 15-28 under 35 U.S.C. § 103(a) as being unpatentable over Current (U.S. Pat. No. 5,155,369) in view of Aitken (U.S. Pat. No. 4,578,589)

Respectfully submitted,

Larry J. Prescott

Larry J. Prescott, Reg. No. 39,335

THE CLAIMS

1. (TWICE AMENDED) A method of forming source/drain regions, comprising the steps of:

providing a semiconductor integrated circuit wafer having source/drain regions;

providing an ion implant apparatus;

placing a phosphorous ion source in said ion implant apparatus;

adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising P_2^+ ions, wherein said ion beam has a beam density and a beam energy;

implanting impurities into said source/drain regions of said integrated circuit wafer, wherein said impurities consist of P_2^+ ions implanted using a single ion implantation step and said ion beam; and

annealing said integrated circuit wafer having P_2^+ ions implanted at an anneal temperature for an anneal time.

2. The method of claim 1 wherein said adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising P_2^+ ions uses a magnetic analyzer.

3. The method of claim 1 wherein said beam density is between about 4×10^{14} and 6×10^{14} ions/cm^2.

4. The method of claim 1 wherein said beam energy is between about 20 and 48 KeV.

5. The method of claim 1 wherein said anneal temperature is between about 900°C and 1100°C.

6. The method of claim 1 wherein said anneal time is between about 10 and 20 seconds.

7. The method of claim 1 wherein said phosphorous ion source comprises solid phosphorous.

8. (TWICE AMENDED) A method of forming source/drain regions, comprising the steps of:

providing a semiconductor integrated circuit wafer having source/drain regions;

providing an ion implant apparatus;

placing an arsenic ion source in said ion implant apparatus;

adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising As_2^+ ions, wherein said ion beam has a beam density and a beam energy;

implanting impurities into said source/drain regions of said integrated circuit wafer, wherein said impurities consist of As_2^+ ions implanted using a single ion implantation step and said ion beam; and

annealing said integrated circuit wafer having As_2^+ ions implanted at an anneal temperature for an anneal time.

9. The method of claim 8 wherein said adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising As_2^+ ions uses a magnetic analyzer.

10. The method of claim 8 wherein said beam density is between about 4 X 10^{14} and 6 X 10^{14} ions/cm^2.

11. The method of claim 8 wherein said beam energy is between about 20 and 48 KeV.

12. The method of claim 8 wherein said anneal temperature is between about 900°C and 1100°C.

13. The method of claim 8 wherein said anneal time is between about 10 and 20 seconds.

14. (ONCE AMENDED) The method of claim 8 wherein said arsenic ion source comprises solid arsenic.

15. (TWICE AMENDED) A method of doping a polysilicon electrode, comprising the steps of:

providing a semiconductor integrated circuit wafer having a polysilicon electrode formed thereon;

providing an ion implant apparatus;

placing a phosphorous ion source in said ion implant apparatus;

adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising P_2^+ ions, wherein said ion beam has a beam density and a beam energy;

implanting impurities into said polysilicon electrode, wherein said impurities consist of P_2^+ ions implanted using a single ion implantation step and said ion [implant] beam; and

annealing said integrated circuit wafer having P_2^+ ions implanted at an anneal temperature for an anneal time.

16. The method of claim 15 wherein said adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising P_2^+ ions uses a magnetic analyzer.

17. The method of claim 15 wherein said beam density is between about 4×10^{14} and 6×10^{14} ions/cm^2.

18. The method of claim 15 wherein said beam energy is between about 20 and 48 KeV.

19. The method of claim 15 wherein said anneal temperature is between about 900°C and 1100°C.

20. The method of claim 15 wherein said anneal time is between about 10 and 20 seconds.

21. The method of claim 15 wherein said phosphorous ion source comprises solid phosphorous.

22. (TWICE AMENDED) A method of doping a polysilicon electrode, comprising the steps of:

providing a semiconductor integrated circuit wafer having a polysilicon electrode formed thereon;

providing an ion implant apparatus;

placing a arsenic ion source in said ion implant apparatus;

adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising As_2^+ ions, wherein said ion beam has a beam density and a beam energy;

implanting impurities into said polysilicon electrode, wherein said impurities consist of As_2^+ ions implanted using a single ion implantation step and said ion [implant] beam; and

annealing said integrated circuit wafer having As_2^+ ions implanted at an anneal temperature for an anneal time.

23. The method of claim 22 wherein said adjusting said ion implant apparatus so that said ion implant apparatus produces an ion beam comprising As_2^+ ions uses a magnetic analyzer.

24. The method of claim 22 wherein said beam density is between about 4 X 10^{14} and 6 X 10^{14} ions/cm^2.

25. The method of claim 22 wherein said beam energy is between about 20 and 48 KeV.

26. The method of claim 22 wherein said anneal temperature is between about 900°C and 1100°C.

27. The method of claim 22 wherein said anneal time is between about 10 and 20 seconds.

28. The method of claim 22 wherein said arsenic ion source comprises solid arsenic.